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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/583,538
Filing Date	June 15, 2006
First Named Inventor	Ralf Brederlow
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	V0195.0080

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA*	US-7,012,468-A1	03-14-2006	Brederlow et al.	
	AB*	US-5,392,043	02-21-1995	Ribner	
	AC*	US-20030128776-A1	07-10-2003	Rawlins et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA	DE-100 01 124-C1 – corresponds to USP 7,012,468 (attached)	06-07-2001	Infineon Technologies Ag		√
	BB	DE-44 35 305-A1 – corresponds to USP 5,392,043 (attached)	04-06-1995	General Electric Company		√
	BC	DE-100 45 148-A1 – translation of abstract only	03-28-2002	Hella Kg Hueck & Co		√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	S. Christensson et al.; "Low Frequency Noise in MOS Transistors - I Theory"; Solid-State Electronics, Pergamon Press 1968, Vol. 11, pages 797-812.	
	CB	R. Brederlow et a.; "Influence of Fluorinated Gate Oxides on the Low Frequency Noise of MOS Transistors under Analog Operation"; Proceedings of the 28th European Solid-State Device Research Conference, pages 472-475, 1998.	
	CC	S.L.J. Gierkink et al.; "Reducing MOSFET 1/*f* Noise and Power Consumption by "Switched Biasing"; Proceedings of the 28th European Solid-State Circuits Conference, pages 154-157, 1999.	
	CD	E. Simoen et al.; "Empirical Model for the Low-Frequency Noise of Hot-Carrier Degraded Submicron LDD MOSFET'S"; IEEE Electron Device Letters, Vol. 18, No. 10, pages 480-482, October 1997.	
	CE	I. Bloom et al.; "1/*f* noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation"; Appl. Phys. Lett. 58 (15), pages 1664-1666, 15 April 1991.	
	CF	R. Gregorian et a.; "Analog MOS Integrated Circuits"; NY, John Wiley & Sons, 1986.	
	CG	P.E. Allen et al.; "CMOS Analog Circuit Design"; New York, Oxford University Press, 1987.	
	CH	P.R. Gray et al.; "Analysis and design of analog integrated circuits"; NY, John Wiley & Sons, 1993.	
	CI	A.B. Grebene; "Bipolar and MOS analog integrated circuit design"; NY, John Wiley & Sons,	

Examiner Signature		Date Considered	

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Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	V0195.0080

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	CJ	J. Tihanyi et al.;"Properties of ESFI MOS Transistors Due to the Floating Substrate and the Finite Volume"; IEEE Transactions on Electron Devices, Vol. ED-22, No. 11, pages 1017-1023, November 1975.	
	CK	M. Chan et al.; "Comparative Study of Fully Depleted and Body-Grounded Non Fully Depleted SOI MOSFET's for High Performance Analog and Mixed Signal Circuits"; IEEE Transactions on Electron Devices, Vol. 42, No. 11, pages 1975-1981, November 1995.	
	CL	B.M. Tenbroek et al.; "Impact of Self-Heating and Thermal Coupling on Analog Circuits in SOI CMOS"; IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, pages 1037-1046, July 1998.	
	CM	A. Wei et al.; "Minimizing Floating-Body-Induced Threshold Voltage Variation in Partially Depleted SOI CMOS"; IEEE Electron Device Letters, Vol. 17, No. 8, pages 391-394, August 1996.	
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	CO	K.A. Jenkins et al.; "Characteristics of SOI FET's Under Pulsed Conditions"; IEEE Transactions on Electron Devices, Vol. 44, No. 11, pages 1923-1930, November 1997.	
	CP	L.M. Perron et al.; "Switch-Off Behavior of Floating-Body PD SOI MOSFET's"; IEEE Transactions on Electron Devices, Vol. 45, No. 11, pages 2372-2375, November 1998.	
	CQ	S.L.J. Gierkink et al.; "Intrinsic 1/*f* Device Noise Reduction and Its Effect on Phase Noise in CMOS Ring Oscillators"; IEEE Journal of Solid-State Circuits, Vol. 34, No. 7, pages 1022-1025, July 1999.	
	CR	E.A.M. Klumperink et al.; "Reducing MOSFET 1/*f* Noise and Power Consumption by Switched Biasing"; IEEE Journal of Solid-State Circuits, Vol. 35, No. 7, pages 994-1001, July 2000.	

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